REMARKS/ARGUMENTS

Claims 2-4 and 6-15 are pending in the present application.

This Amendment is in response to the Office Action mailed April 26, 2004. In the Office Action, the Examiner rejected claims 2-4 and 6-15 under 35 U.S.C. §103(a). Applicants have amended claim 3. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 103

1. In the Office Action, the Examiner rejected claims 2-4 and 6-15 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,636,942 issued to Chen et al. ("Chen") in view of Japan Patent No. JP406232664A issued to Kojiro et al. ("Kojiro"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness. As the Examiner is aware, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Applicants reiterate the arguments set forth in the previously filed Response to the Office Action.

Chen discloses a computer vector multiprocessing control. A central memory is provided for two processors. Each processor has a respective data path and respective control path to the central memory (Chen, col. 4, lines 65-68). The two processors are identical and symmetric (Chen, col. 5, lines 50-51). The central memory is provided with eight ports, with four ports associated with each processor (Chen, col. 10, lines 31-32). There is no storage of real-time audio data associated with audio channels. Chen does not disclose, suggest, or render obvious memory banks storing subsets of audio data corresponding to different groups of audio channels.

Kojiro discloses a mixer. n sets of channel setting information are stored in a channel data bank (Kojiro, Constitution, Figure 1, element 7). N of these n sets are selected from the channel data bank to be stored in N sets of local banks in a routing switcher (Kojiro, Constitution, Figure 1, elements 2, 3_1 to 3_N). These N sets are reproduced to M sets of channels of mixer (Kojiro, Constitution, Figure 1, element 6).

Chen and Kojiro, taken alone or in any combination, does not disclose, suggest, or render obvious: (1) a plurality of memory banks having two memory banks accessible to first and second processors for operations selected from the group comprising read and write operations, and (2) storing subsets of audio data in the memory banks and the subsets corresponding to different groups of audio channels. The combination of Chen in view of Kojiro would teach away from the claimed invention in that it would teach or describe a computer vector multiprocessing with a channel data bank connected to local banks in a router.

There is no motivation to combine Chen and Kojiro because neither of them addresses the problem of memory allocation for real time audio processing. There is no teaching or suggestion that audio data from audio channels, plurality of memory banks, and storing subsets of audio data corresponding to different groups of audio channels are present. Chen, read as a whole, does not suggest the desirability of memory allocation by storing subsets of audio data corresponding to different groups of audio channels.

The Examiner stated that Kojiro disclosed using subsets corresponding to different groups of audio channels. Applicants respectfully disagree. Kojiro merely discloses a technique to mix M sets of input signals based on N sets of channel information. Kojiro does not disclose or suggest memory banks storing subsets corresponding to different groups of audio channels. Kojiro does not disclose or suggest two processors. Even if the mixer is interpreted as a processor, it does not have access to the channel data banks or the local banks by read and write operations. As clearly shown in Figure 1 and stated in the description, Kojiro discloses mixing M sets of input signals using the N sets of channel setting information. The local banks store the setting information, not the subsets of audio data. Furthermore, since these local banks obtain data from the channel data bank, they cannot be real-time data.

Furthermore, combining Chen and Kojiro would render the prior art invention unsatisfactory for its intended purpose. If the proposed modification would render the prior art

invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01.

Here, Chen disclosed a central memory being segmented into thirty-two independently controllable banks (Chen, col. 11, lines 18-20). These banks are organized into four sections, each containing eight banks (Chen, col. 11, lines 20-21). Each of the four sections is provided with two independent access paths, each controlled by one of the CPU's, to the memory banks therewithin (Chen, col. 11, lines 25-28). On the other hand, Kojiro discloses a channel data bank containing setting information to be selected for storing in the local banks. The setting information is not real-time audio data. A mixer mixes input signals using these sets of selecting setting information. Therefore, the channel data bank is read to the local banks and the local banks are read to the mixer, not independently controllable banks as disclosed in Chen.

Modifying Chen to incorporate the channel data banks local banks in Kojiro would render the multiprocessing unsatisfactory for its intended purpose. The intended purpose of the central memory organization in Chen is to provide independent and parallel accesses (Chen, col. 3, lines 44-50). Incorporating the channel data banks and local banks in Kojiro would prohibit independent accesses from the two processors because these banks are not available for accesses by any processors. Furthermore, the local banks obtain setting information directly from the data bank, not from a processor (Kojiro, Figure 1, element 3_1 to 3_N).

Therefore, Applicants believe that independent claims 3, 6 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejection under 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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